Missing Pieces in the Puzzle of Ultra-high Speed All-Optical Logic

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Recent experiments have demonstrated all-optical, digital logic circuits operating at speeds up to 100 Gbps [1,2]. Logic circuits based on semiconductor devices [1,3,4], possess the advantage of low switching energy, low latency which is important in circuits using feedback and the potential for eventual integration and for this reason they may see commercialization before fiber-based devices. Two important issues that must be resolved before autonomous and functional, all-optical, digital logic circuits can be built based on semiconductor devices, are the demonstration of Boolean XOR and a means for gate synchronization. In this presentation we demonstrate Boolean XOR operation at 10 Gbps using an SOA assisted Sagnac interferometer [5] and an optical clock multiplication circuit that may be used for local gate synchronization [6]. The XOR operation of the SOA-assisted Sagnac was verified using two modulated optical control beams A and B that may take a logical 0 and 1. The logical output is imprinted on a third optical beam (CLK) which is held on input continuously to a logical 1 and is monitored at the transmission port T of the gate. Figure 1(a) shows the experimental configuration. The three optical signals were produced from two gain switched DFB laser diodes, LD1 and LD2 driven at 5 GHz and producing 12 ps pulses after linear compression. The optical clock signal (CLK) was provided by LD1 at 1532.8 nm. The pseudo-data pattern for the two logical control inputs was produced from LD2 at 1534.1 nm with a Li:NbO_3 modulator driven from a programmable, 500 MHz pulse generator. The repetition frequency of the clock was doubled to 10 GHz with a split-relative-delay-and-combine fiber doubler. The doubler also served to construct the 10 Gb/s, 16 bit-long pseudo-data pattern. The clock and control signals were amplified in a common EDFA 1 and separated with tunable filters before being launched into the gate input ports.

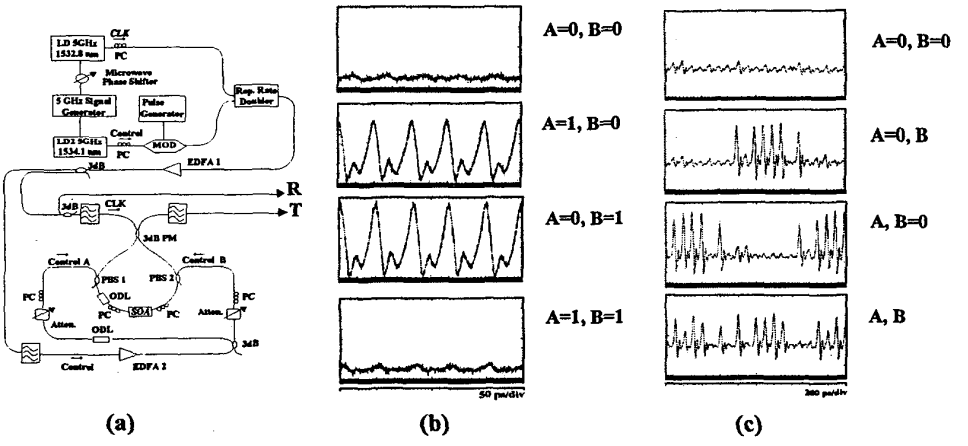

Figure 1 (a) Experimental set up, (b) 10 GHz XOR operation and (c) 10 Gbps XOR operation

The control pulse train was further amplified in EDFA 2 and provided the two control inputs A and B after splitting in a 3 dB coupler. The SOA-assisted Sagnac interferometer gate was constructed using a 3 dB polarization preserving coupler into the ports of which the input-output of the clock signal is injected. Polarization selective fiber couplers (PBS) were used in the loop to couple in and out the orthogonally polarized pulses of the logical control inputs A and B. The nonlinear interaction between the control and clock pulses was performed in a 1000 □m long, bulk SOA with 100 ps recovery time which was offset from the center of the loop by 30 ps for optimum switching. For successful Boolean XOR between A and B, the transmission port T of the gate must record a '1' if either A or B is '1' and a '0' if both A and B are '1'. Figures 1(b) and (c) show the T port output of the gate in the absence and in

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the presence of data modulation respectively for the 4 combination of A and B controls and prove correct XOR operation for the gate. The pulse energy needed for the clock signal was 5 fJ and for the control inputs A and B was up to 80 fJ and 100 fJ respectively.

An all-optical, digital circuit will consist of a small number of interconnected, high-performance, optical logic gates. For operation each gate will require a high speed optical clock, running at a repetition frequency defined by its logical functionality and synchronized to the circuit master clock. Even though it is possible that each local clock is driven and synchronized electrically, this will lead to significant complexity. Figure 2 (a) shows a simple all-optical circuit that may be used as a local clock for an optical logic gate in a circuit and which may be used for repetition frequency selection and synchronization to a master optical clock. The circuit is a mode-locked fiber ring laser that uses a SOA for gain and gain modulation, which is provided from an external optical pulse train.

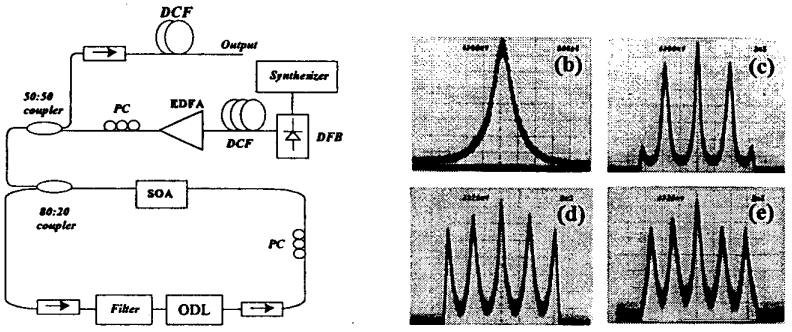

Figure 2 (a) Experimental set up, (b)-(e) output pulse autocorrelation traces at 25, 30, 35, 40 GHz respectively. 1 ms time base corresponds to 8.3ps

Gain in the clock circuit was provided from a 500 □m, bulk InGaAsP/InP ridge waveguide SOA with peak gain of 23 dB at 1535 nm. Faraday isolators ensured unidirectional oscillation in the ring and a 3 dB fiber coupler placed after the SOA was used to insert the external modulating signal and to obtain the output from the source. Wavelength selection in the ring was achieved with a 5 nm tunable filter. The externally introduced pulses were provided from a gain switched DFB laser at 5 GHz operating at 1548.9 nm and which were linearly compressed to 8.3 ps. The mode-locked pulses obtained directly from the multiplier circuit were compressed using a dispersion compensating fiber of total dispersion −11.4 ps/nm placed at its output. The gain modulation in the ring cavity is optical and if the external source is gain switched at a harmonic of the ring, then this mode-locks at the frequency of the external pulses. If however the gain switched pulse train cavity is detuned by □□$_f$/n, where □□$_f$ is the fundamental ring cavity frequency and n is an integer, the ring cavity mode-locks at n times the frequency of the external pulses. Figure 2(b)-(e) shows the autocorrelation traces at the output of the ring oscillator at 25, 30, 35 and 40 GHz respectively. The traces indicate pulse widths of 2.5 ps assuming squared hyperbolic secant pulse profiles. The significant attribute of this oscillator which makes it a good contender as a local gate clock in an all-optical, digital circuit, is that it may mode-lock at a relatively high rate, harmonic to a relatively low rate optical signal to which it is synchronized.

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