Computer Networks 52 (2008) 1873–1890

Contents lists available at ScienceDirect

Computer Networks

journal homepage: www.elsevier.com/locate/comnet

Photonics in switching: Architectures, systems and enabling technologies ☆

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ARTICLE INFO

Article history:
Received 31 May 2007
Received in revised form 17 January 2008
Accepted 6 February 2008
Available online 21 March 2008

Keywords:
Optical networking
Optical switching
Optical switch architecture
Switching experiment

ABSTRACT

This paper describes recent research activities and results in the area of photonic switching carried out within the Virtual Department on Switching (VDS) of the European e-Photon/ONe Network of Excellence. Contributions from outstanding European research groups in this field are collected to offer a platform for future research in optical switching. The paper contains the main topics related to network scenarios, switch architectures and experiments, with an effort to investigate synergies and challenging opportunities for collaboration and integration of research expertise in the field.

1. Introduction

The e-Photon/ONe Network of Excellence (NoE) is a project funded by the European Commission (EC) which aims at integrating and developing knowledge in the field of optical networking and photonic technology [1]. Project activities have been organized around Virtual Departments (VDs) and Joint Project (JP) initiatives. Virtual Departments coordinate the NoE activities on selected broad disciplines, while Joint Projects tailor research activities to specific themes. Optical switching, which is one of the main topics of this project, is coordinated within a workgroup called Virtual Department on Switching (VDS).

The main objective of the VDS is to explore R&D directions and picture the position of photonic switching in future optical networks: how and where photonic switching is positioned in the future Internet. Recent technology

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1389-1286/$ - see front matter
doi:10.1016/j.comnet.2008.02.024

development has unlocked most of the fibre capacity making it an abundant resource. However, the WDM (Wavelength Division Multiplexing) deployment has mainly occurred in the form of point-to-point links with amplifiers in between if needed. Optical WDM lightpaths are static and are seen as a scarce resource. Once set up, they remain in place, essentially forever.

The incentive is to use optical switching to make spectrum efficient in terms of switching and not in terms of capacity only. Towards this goal VDS has charted a list of key issues and prime research objectives. Actual implementation was carried out based on collaborative projects initiated by VDS members. Results of the integration activities were reviewed every year in technical meetings, while the technology impacts and achievements were assessed as well. This further resulted in revisions of the list of key issues identified and potentially contributed to new integrating activities.

In this tutorial paper the main aspects of photonic switching are presented in a system and enabling technology perspective. Recent concepts and subsystems to build an optical switch are described and their practical applications are demonstrated through the presentation of state-of-the-art system experiments. Research results from different partners aim at giving a synergic overview of research effort in photonics in switching in Europe, to show how technology and system expertise could produces successful designs.

The paper is organized as follows. In Section 2 the key techniques for optical networking are introduced and reviewed. In Section 3 recent achievements in enabling technologies are discussed. In Section 4 architectures for optical circuit-switching are described, while Section 5 is devoted to optical packet switched architectures in asynchronous and synchronous contexts. Section 6 surveys the main experiments on optical networking carried out in Europe ranging from hybrid solutions to all-optical switching. Section 7 concludes the work.

2. Key techniques for optical networking

Research in the area of optical networking can be categorized in the near-term as automatically reconfigurable circuit-switching solutions [2], near to long term as optical burst switching solutions [3–5] and long term as optical packet-switching solutions [6–8]. The implementation feasibility of these solutions is reflected in the results of theoretical studies and demonstrations. Optical circuit-switching (OCS) technology is currently moving towards the deployment of fast and automatically reconfigurable nodes with switching granularity at the wavelength level provided by advanced signaling capabilities. This approach is now leading to standards as the Automatically Switched Optical Network (ASON) architecture [9]. ASON networks, which are based on SDH/SONET, assures QoS, management and security.

Due to the domination of IP-centric traffic, future solutions are focusing on bursty networking models able to handle dynamic segments instead of continuous data. Optical Burst Switching (OBS) is designed to offer increased bandwidth utilisation and reduced overhead. A path is dynamically set-up and torn down for the time required to transmit a complete set of data, the 'data burst' [3]. The main advantages of OBS in comparison to the other optical networking schemes are that the optical bandwidth is reserved only for the duration of the burst and that the core network can be bufferless. In any case, OBS needs switch reconfiguration speed in the order of microseconds.

The feasibility of OBS technology has been investigated in a number of reported field trials and testbeds. A quite complete demonstrator with six nodes and MEMS-based switches was set-up in Japan and achieves switching times of 1 ms for bursts with a minimum size of 100 ms [3]. In China an OBS field experiment has been demonstrated with three edge and one core nodes. Node switching time is in the order of nanosecond times using SOA technology. This allowed the assembling of relatively small packets (720 μs), transmitted at 1.25 Gb/s [3]. OBS has been also identified as a compatible solution for the physical layer infrastructure in Grid computing applications, with possible realization on NRENs [2]. Recent achievements in Europe in OBS research were reported in [5].

Optical packet-switching (OPS) is a purely connectionless networking solution that is fully compatible with IP-centric data traffic and offers the finest network granularity and optimum bandwidth utilisation [6]. The main challenges in OPS are the implementation of the optical header processing mechanism, the development of an intelligent switch controller, the realization of ultra-fast switching at a nanosecond timescale and the exploitation of buffering mechanisms to reduce packet blocking. On the other hand, OPS implies higher requisites than OBS because of packet processing on the fly. Existing OPS demonstrators are mainly restricted to the development of fully functional but small switching elements that simply show the feasibility of fast packet-switching on the physical layer with some extensions to the link layer. In the OPSnet project [7] dynamic switching of asynchronous optical packets at 40 Gb/s has been demonstrated in a fully controllable set-up able to identify and process the header and route the payload accordingly. In [8] contention resolution in the wavelength domain is also considered in a 10 Gb/s packet-switching node. Newly developed schemes [11] are based on the same concept and use more advanced electronics for faster clock extraction and processing, while the integration capabilities with the wavelength selective switch are investigated. A more feasible approach towards the implementation of OPS considers the use of synchronously (slotted) transmitted packets with fixed lengths. However, in this case the hardware overhead is on the implementation of the packet synchroniser at the input. Nevertheless, slotted solutions are attractive for other applications like computer interconnects. Despite their feasibility limitations, OPS demonstrators assisted the development of numerous ultra-fast switching and processing techniques regarding wavelength conversion, header encoding/decoding and processing, label swapping, fast clock extraction, regeneration and optical contention resolution [10]. Additionally, various switch architectural designs and control protocols have been proposed, which in combination with the significant technological advances over the last years, indicates the possible deployment of OPS in the future.

Concerning the control plane, the Generalized Multi-protocol Label switching (GMPLS) framework is a promising candidate for optical networks. Current research efforts are aimed at improving its efficiency in various operational contexts. In WDM circuit-switched optical networks, labels correspond to physical wavelengths and the assumption that all available labels are equal as happens in electronic networks is no longer valid. So labels which save wavelength converters (WCs) at optical nodes, or reduce either the physical impairments or the collision with concurrent requests are preferred. Schemes for collecting preferences for specific labels during GMPLS signaling have been proposed in relation to WC usage [10] which can be extended to minimize a wide range of objective functions. This allows for a RSVP-TE-compliant realization of, e.g., physical impairment-based routing or load-balancing.

3. Enabling technology

Through the advent of optical technologies, it has been identified that photonic switching possesses advances over other candidate technologies such as speed, lower power consumption and small footprint [42]. Key subsystems that exploit these benefits are optical buffers, optical multiplexers/demultiplexers and switching fabrics for OPS/OBS/OCS applications. Basic building blocks for implementing these are wavelength converters, optical logic gates and regenerators. Such devices have been implemented and utilized in single-gate experiments performing wavelength conversion at rates over 160 Gb/s or regeneration with bitwise processing capability in excess of 40 Gb/s [35]. In this way they offer a feasible platform for high-speed processing required by future circuit-switched nodes. However, much of the research in wavelength conversion and regeneration configurations has been focused on continuously increasing processing speed performance of optical gates and not on exploring their logic and functional potential.

The evolution from fibre-based single-gate experiments to more complex all-optical subsystems has been made possible due to the development of compact SOA-MZI-based optical gates and flip-flops, which exploit the integration capabilities of hybrid technology. Hybrid integration is uniquely designed for passive assembly of the different components in order to maintain high optical performance and low insertion losses, but at a much lower cost. In a similar manner as the electronic printed-circuit board used in electronics, a planar silica on silicon waveguide acts as a motherboard to host both active and passive devices. Integration is achieved by plugging precision-machined silicon submounts or "daughterboards" carrying individual optical components into the motherboard. The individual components have precision cleaved features for accurate mechanical positioning on the daughterboard.

The first milestone on the development of all-optical subsystems is reached by verifying that discrete, yet integrated and compact, all-optical gates can be interconnected to produce all-optical circuits with increased functionality and intelligence. The next milestone involves the integration of generic optical gates on the same hybrid platform, in order to reduce packaging costs and increase the photonic integration level.

The next logical step, on this migration path, lies at the photonic integration level. Next generation photonic devices must include on-chip interconnections and integration of different optical components on a single chip [43,44]. Key components that should be co-integrated include ring resonators for optical filtering applications, wavelength converters and MZI-SOA based subsystems for packet processing applications.

3.1. Ring Resonator technology

These filters can be implemented in optical fibre technology (microloops) and in the silicon or InP integrated optic technologies. Photonics circuits with equivalent components have already been developed [45]. Some of them are a monolithically integrated Sagnac interferometer for an all-optical controlled-NOT gate, filters using active ring resonators, passive single and double ring resonators and micro-cavities. The resonant frequencies of the proposed device can be shifted by changing the equivalent loop length by carrier injection, or local heating as in any ring resonator based device. The transfer function can be tailored by changing the loop loss; with specific choice of materials (III–V) for fabrication, the electro-absorption effect can be used for this purpose. The filter resonant frequencies can also be changed by tuning the coupling ratio. Nowadays, this is technologically feasible (i) by adjusting the taper–resonator gap fabricated by stretching a standard optical fibre, (ii) with a micromechanical fibre variable ratio coupler, using MEMS actuated deformable waveguides [46], or (iii) using electrical control of waveguide resonator coupling in a MZ coupler configuration [47].

3.2. Wavelength converters

Wavelength conversion has been considered a basic function for a variety of applications spanning from wavelength routing in all-optical networks to contention resolution in all-optical packet/burst switching. The basic operating principle in all wavelength conversion schemes is the exploitation of the physical properties of a nonlinear element to perform a logic function. The main nonlinear elements are SOAs, EAMs, nonlinear fibres and photonic crystals and periodically poled $LiNbO_3$ waveguides (PLLN). SOA based devices and EAMs have the added advantages of compactness and low energy consumption to trigger nonlinearities. Fibres have an instantaneous response to pulses but also limited nonlinear effects, requiring the use of long fibre lengths, which in turn increases the power loss and size of the converter. PLLN based converters require intermediate lengths, while very fast conversion in PLLN structures has been reported. The predominant schemes for wavelength conversion include Cross-Gain/Absorption Modulation (XGM/XAM), Cross-Phase Modulation (XPM) and Four-Wave Mixing (FWM) [48–50].

A newly advanced technology that promises multi-wavelength processing capabilities is Quantum Dot SOAs (QD-SOA) [51]. This capability originates from the physical properties of quantum dots that offer significant advantages over the conventional bulk and even quantum-well based SOA devices. The spatial isolation of dots leads to spectrally localized effects and thus to crosstalk suppression between WDM channels under gain saturation conditions. On the other hand, wavelength channels that have a similar energy level present a strong interaction leading to an effective cross-gain modulation (XGM) of the saturated gain which can be utilized for switching operation when channels are within the homogeneous broadening of the single-dot gain.

3.3. MZI-SOA subsystems

The development of compact SOA-MZI-based optical gates, exploiting hybrid integration allowed the evolution from single-gate experiments to more complex all-optical subsystems. A number of subsystems have been developed and demonstrated, including Clock and data recovery (CDR), label/payload separation and optical buffering, which are critical subsystems. Fig. 1 shows a block diagram of the basic functionalities required to realize an all-optical packet-switched node, namely wavelength conversion, bit-level synchronization, buffering via time-slot-interchanging, regeneration, label processing and packet-switching. The clock recovery subsystem performs bit-level synchronization, while the CDR is performed with 3R regeneration of the incoming traffic [52]. On the other hand, the Label/payload separation subsystem is used to forward the extracted label to the label processing unit and the separated payload to the switching matrix. The Time Slot Interchanger circuit is used to buffer packets and resolve contention. Optical buffering has been investigated in a plethora of architectures that incorporate optical switches and feed-back and feed-forward fibre delay lines, and recent advances in optical integration have enabled the demonstration of an integrated optical buffer.

The first two circuits have been built with three generic, hybrid integrated, MZI switches and a fibre Fabry-Pérot filter, while the latter has been implemented using a quadruple array of SOA-MZI switches of hybrid integrated on a single chip [53].

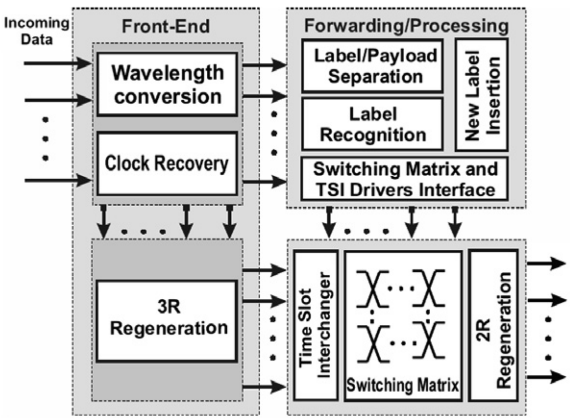

Fig. 1. Top-level design of an all-optical packet-switching node.

The successful integration of the above mentioned devices, will pave the way towards a functional all photonic system on a chip reducing both packaging, pigtailing costs, whilst retaining cost-effectiveness. With the advent of monolithic technology towards the development of larger monolithic chips, it will be possible to constantly upgrade the fundamental active element of the developed photonic platforms, and thus increase the chip integration scale and density. This will eventually lead to increase of integration density, more complex on-chip functionality, and further cost reduction.

4. Circuit-switching architectures

In wavelength-routed networks switching is performed through Optical Add/Drop Multiplexer (OADM) [12] and Optical Cross Connect (OXC) nodes while routing and management of the traffic are applied through GMPLS [10].

OADMs provide capability to add and drop traffic at sites supporting one or two fibre pairs reducing the number of unnecessary optoelectronic conversions. They operate in either fixed or reconfigurable mode. Reconfigurable OADMs (ROADMs) are more complicated but more flexible structures.

The two most common examples of fully reconfigurable OADMs, i.e., "Wavelength Selective" (WS) and "Broadcast and Select" (B&S) architectures are illustrated in Fig. 2a and b. The WS architecture utilises wavelength de-multiplexing/multiplexing and a switch fabric interconnecting all express and add/drop ports, while the B&S is based on passive splitters/couplers and tuneable filters. Fig. 2c illustrates the OSNR evolution across a system supporting different numbers of OADMs based on the two architectures. The analysis is assuming 80 km amplifier spans (20 dB loss) and 6 dB noise figure for all amplifiers used. In addition, the B&S design offers superior performance in terms of filter concatenation effects.

OXCs are located at nodes cross-connecting a number of fibre pairs and support add and drop of local traffic. To offer flexible path provisioning and network resilience, they normally utilise a switching fabric for routing of any incoming channels to the appropriate output ports. In terms of technology, OXCs can be opaque or transparent. Opaque OXCs are either based on electrical or optical switch fabrics surrounded by OEO interfaces. In OXCs using electrical switching, depending on the technology and architecture, sub-wavelength switching granularities can be supported providing edge and intermediate grooming capabilities for more efficient bandwidth utilisation. Opaque OXCs also offer inherent regeneration, wavelength conversion and bit-level monitoring. In transparent OXCs the incoming signals are routed transparently through the optical switch without optoelectronic conversions. The switching granularity may vary between fibre, wavelength band or wavelength channel level. Transparent nodes do not support regeneration capabilities and may significantly impact the scalability of the overall solution

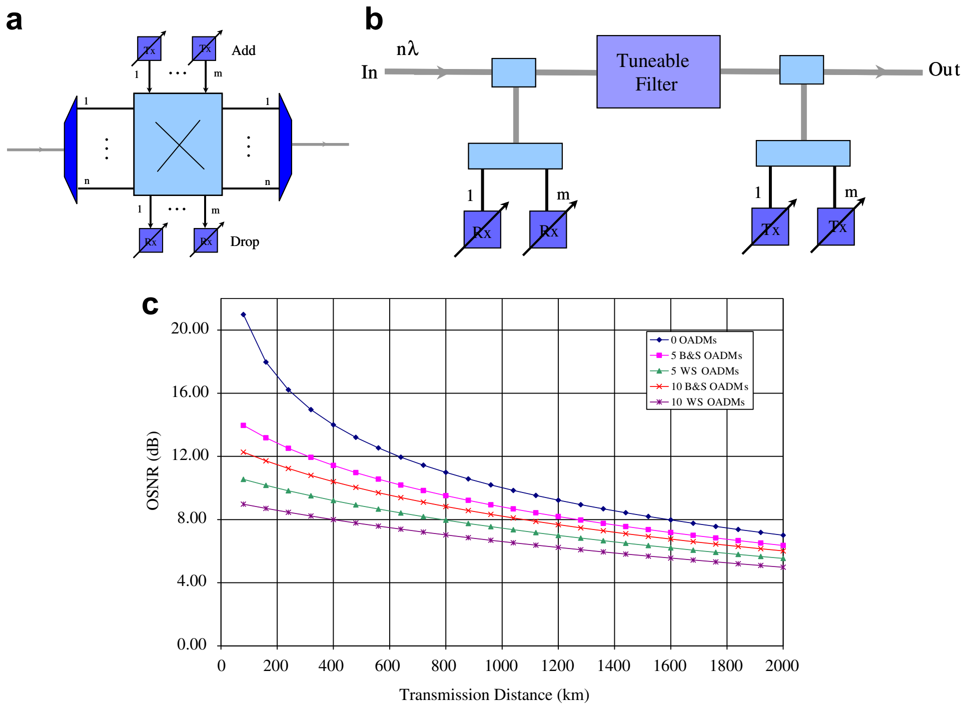

Fig. 2. System OSNR performance. (a) WS OADM architecture; (b) B&S OADM architecture.

as present optical networks are analogue in nature and both transmission and switching introduce impairments. To overcome this, partially regenerating architectures have been proposed. These provide the ability to selectively regenerate individual channels of degraded signal quality through a set of regenerators that can be selectively accessed. Full and partial wavelength conversion can also be applied to reduce wavelength blocking, offer improved bandwidth utilisation and support a control plane scheme compatible with GMPLS. All-optical solutions offer transparency to the signal bit-rate and format. However, different bit-rates and modulation formats may exhibit different transmission characteristics and impairments affecting the overall network design and implementation.

A variety of optical switching technologies has been proposed and developed to date, such as: 2D and 3D MEMS, bubble jet, SOA gates, holographic switches, liquid crystal, thermo-optic, electrooptic technologies and a number of different OXC architectures have been reported [13].

The system concatenation performance of OADMs and OXCs is determined by a number of parameters such as the OSNR, the crosstalk performance, the filtering characteristics of the node, etc. Fig. 3 illustrates that severe power penalties may be introduced in the presence of interferometric crosstalk in the system. Other effects that may cause significant penalties in an optical network are abrupt changes in the traffic loading conditions. In a long chain of amplifiers a change in the spectral loading introduced by adding or dropping in OADMs or switching in OXCs may cause gain tilt and severe transient effects as rapid variations of the amplifier input power level may cause an unwanted sudden gain increase. This problem is commonly overcome using, fast amplifier gain control, gain clamping, Raman amplification or dynamic spectral loading schemes.

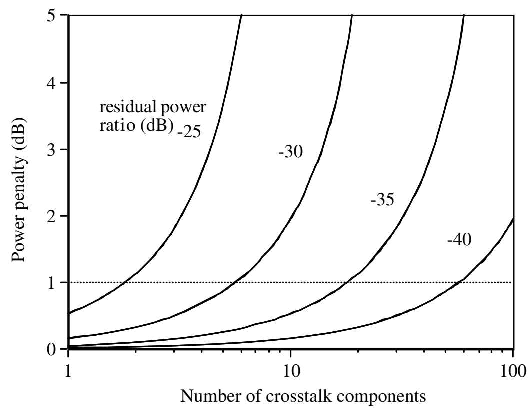

Fig. 3. Power penalty vs. number of crosstalk elements.

4.1. MEMs-based solutions

Here an example of an optical switch based on the so-called 2D MEMS technology is given [14], in which free-space optical beams propagate in a plane parallel to the substrate plane of the fabric. Most 2D MEMS fabrics are designed according to the crossbar architecture. Here 2D MEMS multi-stage architectures based on the classical Benes topology are presented [15,16]. The elementary 4x4 MEMS-Benes Network (MBN) block, the starting architecture from which a MBN of any size can be obtained by recursion, is represented in Fig. 4. The figure also depicts the equivalent Benes network, according to the classical representation. The MEMS device is seen from above the substrate: the electromechanical micro-mirrors are represented by segments corresponding to their vertical position. The optical beams enter the switch from the left side and propagate in a free-space plane parallel to the substrate.

Mirrors are all oriented so that the reflecting plane of each makes a 45° angle with the propagation direction of the optical beam: thus beams are right-angle deflected upon each reflection. The optical beams all leave the switch from the right side. The six 2×2 switching elements (labelled from A to F) are implemented in the MBN by six Movable Mirrors (MMs). A bi-univocal correspondence can be established between Switching Element (SE) and MM states which can be maintained for all the mirrors and for MBNs of any size. The bar SE state corresponds to the laying-down position of the mirror (mirror set parallel to the substrate and not interfering with the beam); the cross SE state corresponds to the tilted-up position of the MM (reflecting surface orthogonal to the substrate and deviating a beam). The MBN also contains Fixed Mirrors (FMs) (represented by a thin segment in the figures): these mirrors have the purpose of steering the beams towards specific locations of the switch, for example steering them to leave the device from the same side and in the correct order. The one-to-one correspondence between SEs and MMs allows the connection routing algorithms to be adopted inside the MBN to be very simply inferred from the algorithms developed for the traditional Benes network. Given an input–output permutation requested from the MBN, the well-known looping algorithm, derived from the classical Benes representation, can be applied to decide the state of each SE. The state of the micro mirror in the MBN is then simply set according to the state of its corresponding SE in the classical Benes. Fig. 4 also shows an example of routing across the 4×4 MBN: there are two connections requested, one from I2 to O3 and the other from I3 to O1. The 4×4 Benes is also represented according to the classical method, supporting the same connections: the functional correspondence between MSN-MMs and SEs is clear.

In [17] the main physical parameters of the MEMS-Benes architecture (size, substrate-area occupation, number of micro mirrors, maximum optical-path length, and maximum number of reflections) have been analyzed. The study shows that the MEMS-Benes feasibility is compatible with the current 2D MEMS technology at least up to a port-count of 64. The main advantage of the new MEMS Benes implementation is still its high scalability in terms of number of movable mirrors: in the case $N = 64$, for instance, the MEMS Benes requires 11 times fewer switching mirrors than the corresponding crossbar fabric.

4.2. SOA based solutions

Multi-stage architectures help to overcome some limitations of single-stage optical cross-connects which require either a large number of space switching elements or tunable wavelength converters that are tuned over a large number of wavelength channels. Both these approaches do not scale easily. A sample switch which employs fast optical technology with tuning speed within the fraction of a microsecond, expected to become a mature option in the near future, was presented in [18]. Scheduling algorithms are typically associated with these structures to assign switch resources.

This multi-stage S–λ–S switching node is presented in Fig. 5. The node consists of N input/output fibres each one carrying M wavelengths and it is organized into three stages. The first and third stages (S) are identical. These space switches exploit the B&S principle and were reported for the first time in [20]; since then they have been extensively considered in literature. The principle of operation is the following: at each node input, after optical amplification by means of an EDFA (Erbium-Doped Fibre Amplifier), a power coupler is used to generate multiple copies of the multi-wavelength bundle of channels entering the node from this input. The power coupler should have $N + 1$ outlets where one outlet per incoming fibre is reserved for a local drop (this outlet is not shown in Fig. 5), while N outlets are directed to a group of N wavelength selectors (WSs). Each WS consists of two grating Mux/Demuxes in tandem (or any device with equivalent functionality) separated by an array of M optical devices that are able to operate as a 'shutter' (on/off gate).

At the output side, the WSs are interconnected by means of a N:1 power combiner in such a way that only one WS from an input fibre might be coupled to an output power combiner. Again, there might be $N + 1$ branches in the coupler to serve for local add. Switching is achieved when the optical device is turned to the on-state, letting

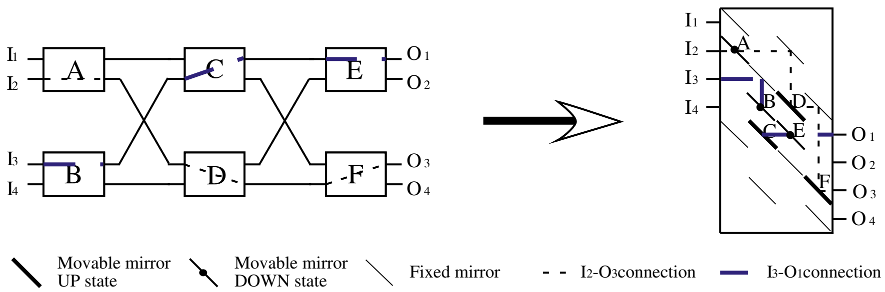

Fig. 4. 4×4 MEMS-Benes network: the elementary block. The optical paths of two connections are displayed.

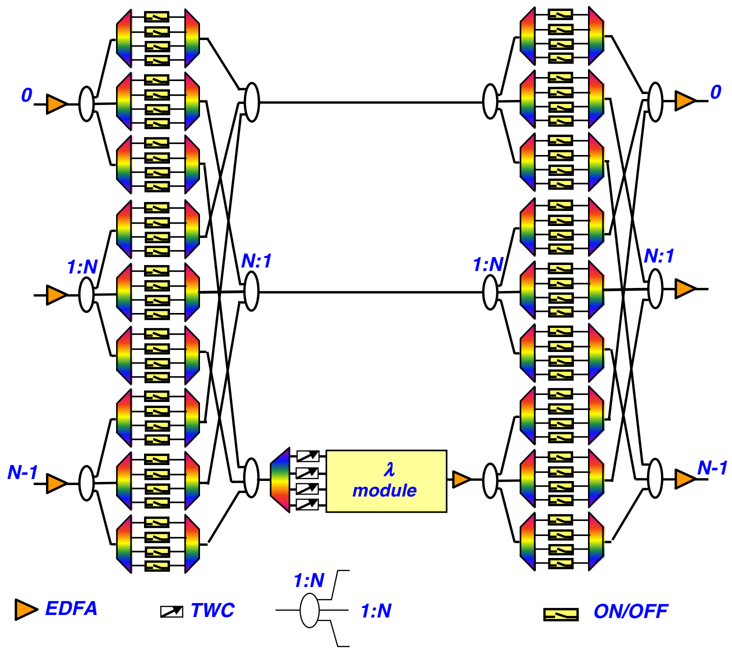

Fig. 5. Multi-stage switching node architecture with $N = 3$ input/output fibres, $M = 4$ wavelengths per fibre with sparse TWCs shared per node.

the wavelength pass through, whilst when a particular wavelength should not be forwarded, it is blocked by switching off the appropriate the gate.

The on-off ratio of the gate determines the level of in-band/out-of-band crosstalk [21]. Since the architecture belongs to the B&S family of switching fabrics it easily allows broadcasting and multi-casting. It is functionally equivalent to M stacked crossbars. The intermediate stage (λ) is composed by N–B optical fibres with M optical channels each and B blocks consisting of an array of M Tunable Wavelength Converters (TWCs) interfaced to the λ-module.

This module can be physically constructed from a variety of devices/subsystems, e.g., (a) an M:1 power coupler (b) an $M \times K$ passive Arrayed-Waveguide Grating AWG router and K:1 coupler (c) an $M \times M$ passive router and an array of M fixed wavelength converters followed by a grating multiplexer. The role of the λ-module is to group all the M wavelengths to a single fibre. Although the options (a–c) are identical in terms of logical performance, their physical layer performance is radically different. Further, the cost difference between these three options is enormous.

At the intermediate stage, each TWC has a different input wavelength, so the proposed architecture may work with either tunable–input tunable–output or fixed–input tunable–output TWCs. Hence, incoming packets carried by the same wavelength (up to N) can exploit N–B optical channels without TWC and B TWCs placed in B different blocks. The proposed switch can be used in virtual wavelength path (VWP) networks offering both shared wavelength path (SHWP) and scattered wavelength path (SCWP) functionality which according to [18] means wavelength-to-wavelength and fibre-to-fibre switching, respectively.

Different heuristic scheduling algorithms can be adopted with the aim to find a compromise between computational complexity and switch performance [19]. The S–λ–S architecture can be used to implement an all-optical switching node with limited number of expensive optical components, both TWCs and SOAs. The number of TWCs employed as well as the value of M (number of wavelengths per fibre) is related to the loss performance expected for the switch. Differently, the number of SOAs employed is independent of the number of TWCs needed, which is an advantage of this proposed architecture. In addition, the number of SOAs needed is a linear function of the number of wavelengths per fibre M.

5. Packet-switching architectures

One of the recognized key issues in OPS design is contention resolution, intrinsically related to any packet-switched system. It is well known that optical switches can exploit the wavelength domain to face this problem, in addition to time and space domains [19,29]. The enabling component for wavelength conversion is the TWC. Its application to solve contention in the wavelength domain has been widely studied [22]. Two different schemes based on tunable wavelength converters shared within the output interface (shared-per-link) or within the entire node (shared-per-node) are proposed, both equipped with a multi-fibre interface [25,26].

Contention resolution in the time domain has been considered as the transposition of the queuing concept in optics. Anyway this approach has some peculiarities that are different from the electronic contexts, being the queueing function implemented by means of a finite number of delays, using fibres, the so called fibre delay lines (FDLs)

[23]. It is shown to be possible to coherently store an optical pulse using electromagnetically induced transparency (EIT). This has been successfully demonstrated at visible wavelengths using atoms as the storage medium [28]. However, most atoms have their principal transitions in the visible or ultra-violet spectrum making them unsuitable for applications in optical communication. Fortunately, we have recently noticed that the Lutetium atom has its principal transition at telecom wavelengths, i.e., around 1337 nm, and can therefore be used as an all-optical buffer in a network switch. The coherence properties of this atom should allow storage times up to 10–20 μs with little pulse degradation.

An example of how to combine different contention resolution schemes in the same optical packet switch, trying to exploit the advantages arising from the interactions among these different approaches, was presented in [26]. A new approach for solving the problem with optical buffering is presented in [27] by proposing an optical asynchronous packet-switch architecture based on electrical buffers. This switch architecture offers the following benefits:

- The advantages of optical switching are combined with the flexibility of electrical buffering.
- The switching node is simple and based on passive, commercially available components ensuring high hardware reliability.
- Packet loss probability can be simply reduced by incrementally adding buffer space.

The benefits of implementing a couple of optical buffer positions in addition to the electrical ones have been investigated. The considered node architecture is shown in Fig. 6. Control functions, such as header processing and switch control, are still performed in the electrical domain [24]. In order to extract information from the headers, the optical signal on each input fibre is initially wavelength demultiplexed and then split into two parts. One part goes to the optical switching fabric while the second is detected at the ingress of the switch control block, where the header is processed. The control block is in charge of the optical switches and buffers (both electrical and optical). The signal, which goes to the switch fabric, is first delayed by fibre delay lines to provide a fixed delay equal to the time taken to process the header and for controlling the switching fabric. The buffer blocks consist of a number of optical buffer positions and twice those much electrical buffers.

A shared recirculation buffer is provided, which allows for reducing buffer size and decreasing packet loss probability. It is based on hybrid buffering, which means that electronic buffer can be added if the optical buffering is insufficient. In this case OEO wavelength conversion within the buffer blocks can additionally improve performance of the switch.

Switch performance has been evaluated through a computer simulation tool that allowed simulations of ATM (Asynchronous Transfer Mode) and IP traffic. We proposed to add a few all-optical buffer positions to the electrical buffer block and evaluated the switching node based on the shared hybrid buffer. We studied the admission

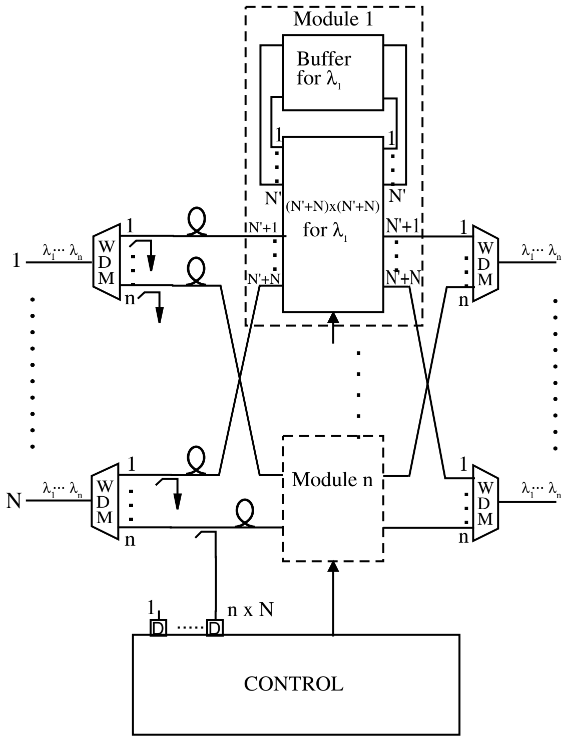

Fig. 6. Node architecture with recirculation shared buffer.

algorithm giving a priority to the service that requires optical signal transparency in order to minimize the time a "transparency" packet has to spend in the buffer. We assumed that the load of this class of packets is 20% of the total load. The transparency packets were scheduled to be transmitted before the packets that could wait in the electrical buffer. In order to avoid starvation of non-priority packets, the transparency packets did not get the "total" priority. Simulation results are presented in Fig. 7. For these simulations maximum storage time in the optical buffer is assumed to be 1 μs. It is shown that the packet loss probability (transparency class) decreases as the buffer size increases until a certain number of buffer positions, which depends on the traffic load and traffic format (ATM or IP). Then, the increase of buffer size does not cause further improvement of the switch performance. This is because the maximum storage time in the optical buffer sets a limit on the waiting time and packet expires in the buffer if the waiting time exceeds this limit. The packet loss probability for ATM traffic is lower than for IP traffic because IP packets can be much longer than ATM cells and the variable delay in optical buffer can be changed up to a certain bound.

In synchronous slotted OPS networks, packets are of a fixed size and have to be aligned at the inputs of the switching node by means of optical synchronization stages. Two types of switching fabrics have been compared: (i) output buffered (OB) switches (i.e., the KEOPS switch [23]) and (ii) Input-Buffered Wavelength-Routed (IBWR) switches [30]. Fig. 8 displays the original IBWR architecture adapted to operate in a WDM network, with

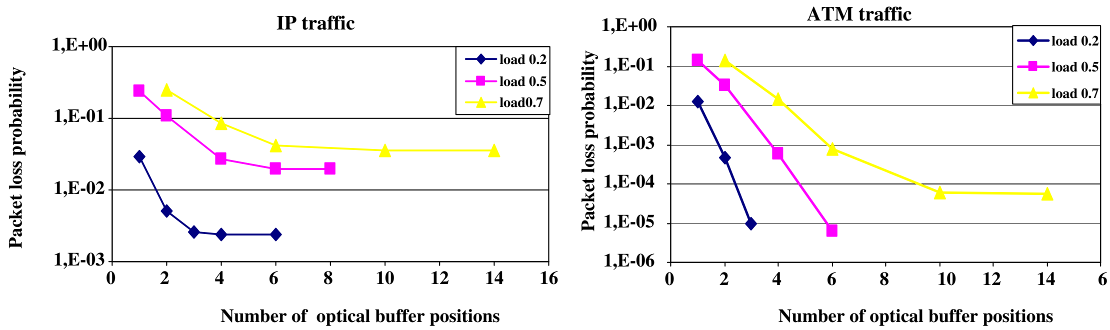

Fig. 7. Packet loss probability for a different traffic load as a function of buffer size (transparency service).

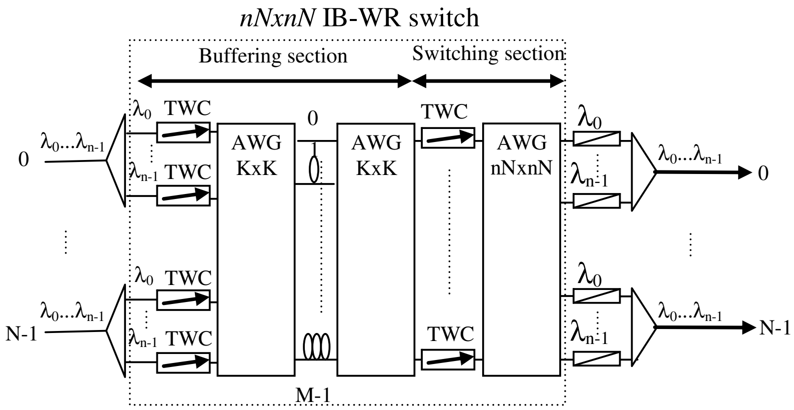

Fig. 8. IBWR switching architecture.

N input/output fibres and n wavelengths per fibre. This means nN input and output ports to the switch. The IBWR switch consists of a buffering section (with M delay lines) connected to a non-blocking switching section. The routing properties of AWG devices make packets from input port i leave the buffering section at the ith output port, independently of the wavelength conversion applied. Wavelength conversion is then used to determine the delay line the packet will go through. The switching section routes the packets to the appropriate output port of the switch. Internal contention arises in the IBWR switch, as two packets arriving at the same input port in different time slots, cannot be scheduled to leave the switch in the same time slot. This is because they would collide in the TWC of the switching section, since TWC devices can operate with only one packet at a time. In [30] it was shown that the underlying delay assignment problem can be modeled as a matching problem in bipartite graphs.

OB architectures provide the optimum throughput performance preserving packet sequence. IBWR switches have an inherent performance penalty because of internal contention. However, IBWR architectures imply a lower cost and better scalability of its hardware. Therefore, a cost vs. performance trade-off arises. To explore this trade-off the IBWR switch is evaluated with two parallel schedulers: (i) I-PDBM [31] scheduler, which does not preserve packet sequence, and (ii) OI-PDBM scheduler [32], which preserves packet sequence at a cost of adding a further

Table 1
Buffer requirements (OB/I-PDBM/OI-PDBM). Under uncorrelated input traffic, to achieve 10^{-7} packet loss probability, $N = \{2,4\}$, $n = \{2,8,32,64\}$

Switch size	$\rho = 0.1$	$\rho = 0.2$	$\rho = 0.3$	$\rho = 0.4$	$\rho = 0.5$	$\rho = 0.6$	$\rho = 0.7$	$\rho = 0.8$	$\rho = 0.9$
$N = 2, n = 2$	2/2/2	3/3/3	3/3/3	4/4/4	5/5/5	5/6/6	7/8/8	10/10/14	18/20/30
$N = 2, n = 8$	1/1/1	2/2/2	2/2/2	2/2/2	2/2/2	2/2/2	3/3/3	3/4/4	6/8/9
$N = 2, n = 32$	1/1/1	1/1/1	1/1/1	1/1/1	2/2/2	2/2/2	2/2/2	2/2/2	2/3/3
$N = 2, n = 64$	1/1/1	1/1/1	1/1/1	1/1/1	1/1/1	1/1/1	2/2/2	2/2/2	2/2/2
$N = 4, n = 2$	3/3/3	3/4/4	4/4/4	5/5/5	6/6/6	7/8/8	9/11/11	14/16/20	26/30/30
$N = 4, n = 8$	1/1/1	2/2/2	2/2/2	2/2/2	2/2/2	3/3/3	3/3/3	4/5/6	8/10/13
$N = 4, n = 32$	1/1/1	1/1/1	1/1/1	1/1/1	2/2/2	2/2/2	2/2/2	2/2/2	3/3/5
$N = 4, n = 64$	1/1/1	1/1/1	1/1/1	1/1/1	1/1/1	2/2/2	2/2/2	2/2/2	2/2/3

performance penalty. Both schedulers allow a parallel electronic implementation, providing a response time independent from switch size.

Table 1 collects the comparative results obtained. It shows buffer requirements for a packet loss probability of 10^{-7} under uncorrelated traffic for three cases: (i) output-buffered architectures, (ii) IBWR architecture without and (iii) with packet sequence preservation. Simulation length is of 10^9 packets. Results show that the buffering requirements gap is small between OB and IBWR architectures, especially in the Dense WDM case. Thus, results endorse the IBWR architecture as a feasible competitor against less scalable OB architectures.

6. System experiments

We present three notable experiments carried out by European groups, to illustrate how optical networking is coming into practical reality.

6.1. Optics inside electronic packet switches: the OSATE project

The research community considers that an early penetration of advanced optical switching technologies is feasible inside electronic packet switches [33,34]. An optical interconnection architecture was originally conceived, studied and prototyped as a network architecture for the metro area. By using simple and commercially available electronic and optical components. A passive WDM all-optical data path over a folded bus is considered as depicted in Fig. 9. The folded bus conveys W wavelengths which first traverse the transmission (TX) bus and, after a folding point, the reception (RX) bus. Each of the N line cards attached to the bus is equipped with one transmitter and one receiver operating at the data rate of a single WDM channel. The input and output ports of the line card are passively coupled to the TX bus and RX bus, respectively. Since full connectivity between all available line cards must be provided on a packet-by-packet basis, fast wavelength tunability at transceivers is required to temporally allocate all-optical single-hop bandwidth. To decrease hardware cost, only transmitters have tuning functionality,

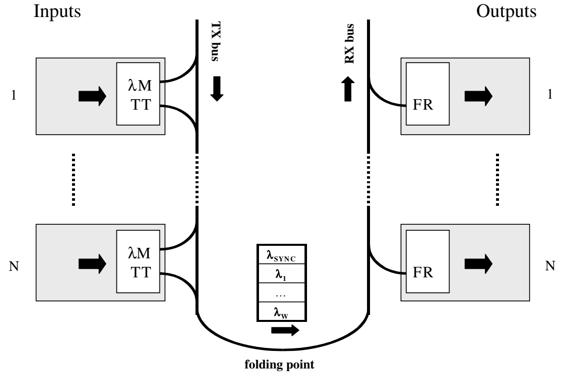

Fig. 9. Node architecture.

while receivers are permanently tuned to a specific WDM channel. When a single receiver per WDM channel is present, and thus the number of available WDM channels W equals the number of line cards N, the architecture can be shown to be equivalent to a distributed crossbar switch, which is able to connect at every time up to N disjoint input–output pairs.

The architecture is synchronous, with time slotted operation. For this purpose, one additional wavelength is dedicated to the distribution of synchronization information along the data path from the first input port to the last output port. As a result, each line card, as shown in Fig. 10, is equipped with one tunable transmitter (TT), which can also include the synchronization transmitter, and one fixed receiver (FR) operating as a burst mode receiver, which drops the synchronization signal to facilitate clock and data recovery.

The slotted behaviour also facilitates the use of distributed scheduling mechanisms, which avoid packet collisions by means of a void-detection mechanism or λ-Monitor (λM) by which line cards know which wavelengths were not used by upstream line cards in each time slot. Priority is given to in-transit traffic, thus without requiring any packet buffering for in-transit data, as well as no packet-switching or stripping in the optical domain.

The TT is used to insert packets in free time slots on the wavelength leading to the packet's destination. The FR always receives all packets on its assigned wavelength. Since output always receive packets on the same wavelength, thus in a non-overlapping way, receiver contention does not occur, since it is solved at the transmitter side. Head-of-the-Line (HoL) blocking is avoided since Virtual Output Queuing (VOQ) is envisioned at inputs; thus, line cards queue packets to be inserted on a per destination-wavelength basis. Since neither packet collisions nor receiver contention occur, transmitted packets are never lost except for transmission errors in the physical layer. The arbitration scheme is based on distributed protocols described in detail in [36] that exhibit high throughput and bounded delay.

The proposed architecture has been demonstrated experimentally at Politecnico di Torino and it is the outcome of former Italian projects RINGO (2000–2001) and WONDER (2004–2005). Currently, a new project dubbed OSATE contemplates the building of a switch prototype based on this architecture. The prototype will be equipped with Gigabit Ethernet cards. The interfaces between Ethernet cards and the optical bus are implemented using development boards with programmable logic (FPGA). The optical bus will make use of WDM to convey multiple channels at 1 Gb/s, and each channel will be shared among all Ethernet cards willing to send incoming packets through the optical bus. The foreseen goal is to build a switch prototype with at least four Gigabit Ethernet interfaces.

6.2. Optical packet-switching node with OEO packet header processing: the WASPNET approach

An example of an OPS node with OEO treatment of the packet label is proposed in the WASPNET project. The OPS

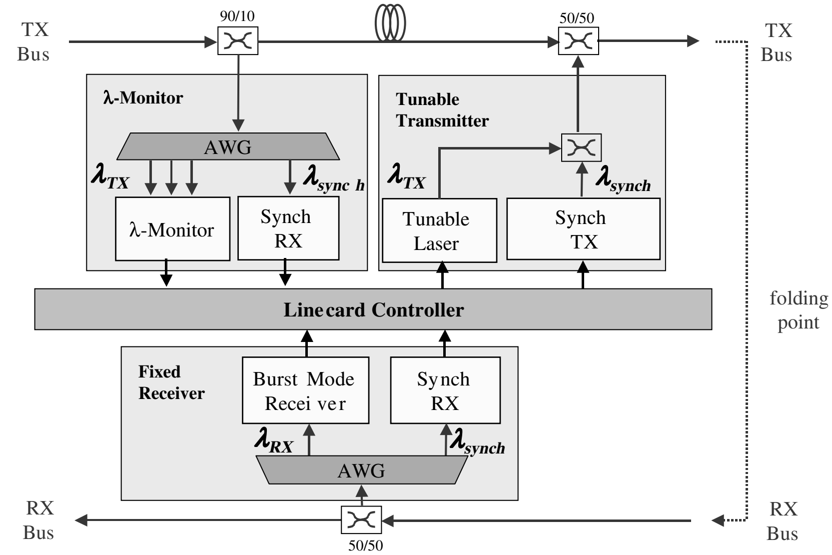

Fig. 10. Line card architecture.

node consists of an F-fibre multi-plane architecture as shown in Fig. 11.

Each plane performs the routing and buffering tasks for packets arriving on a particular wavelength. Fig. 11 also shows the detailed architecture of each wavelength plane. It broadly comprises two stages of processing. In the first stage, the input ports are connected through wavelength converters to an $F \times F$ arrayed-waveguide grating (AWG) which provides contention resolution and routes the packet payload to the correct output port. The second stage comprises wavelength converters followed by an $F \times F$ space switch, which ensures that each packet is switched to the correct output fibre at the proper wavelength. In the cost study of this paper, this node will be referred to as the Node with Electronic Header Processing (NEHP).

The incoming optical packets are first wavelength-demultiplexed and then fed to the corresponding plane to be processed. As an optical packet enters the plane its label is separated and processed electronically. The routing information inside the label controls the fast tuneable input wavelength converter, which then assigns an appropriate wavelength to the packet payload. The payload entering the AWG is passively routed to the appropriate output port according to its wavelength. At the output a further stage of wavelength conversion ensures that the output packet wavelength matches the external network

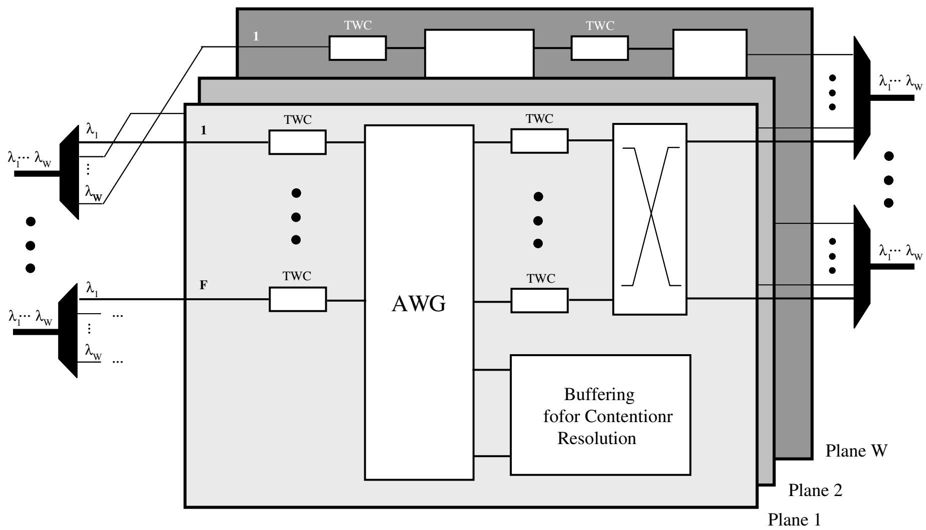

Fig. 11. Architecture of the AWG based switch proposed in WASPNET.

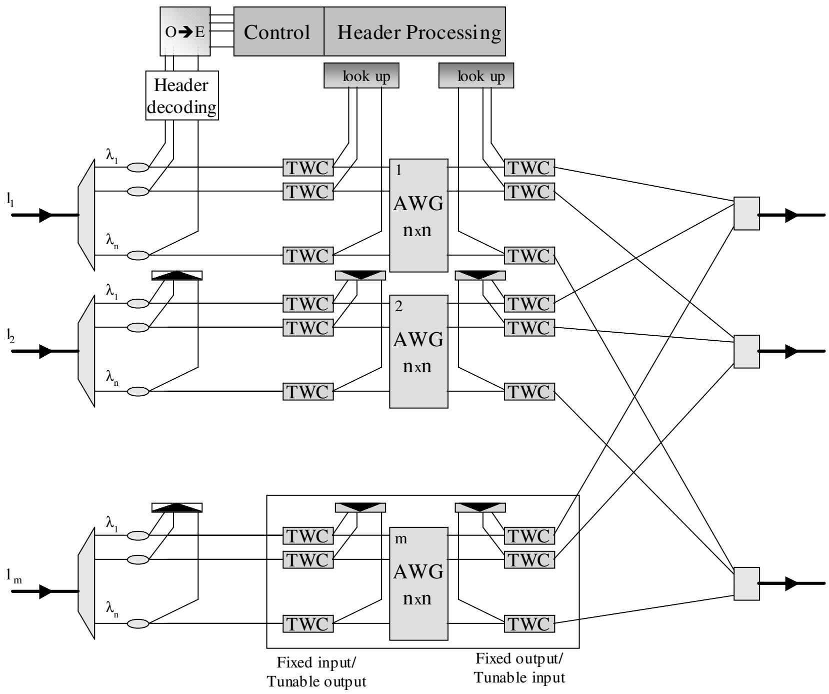

Fig. 12. The OPSnet optical packet switch architecture, a wavelength modular design that supports additional wavelengths per input fibre by adding another switching element. Switching is performed based on wavelength conversion and selection.

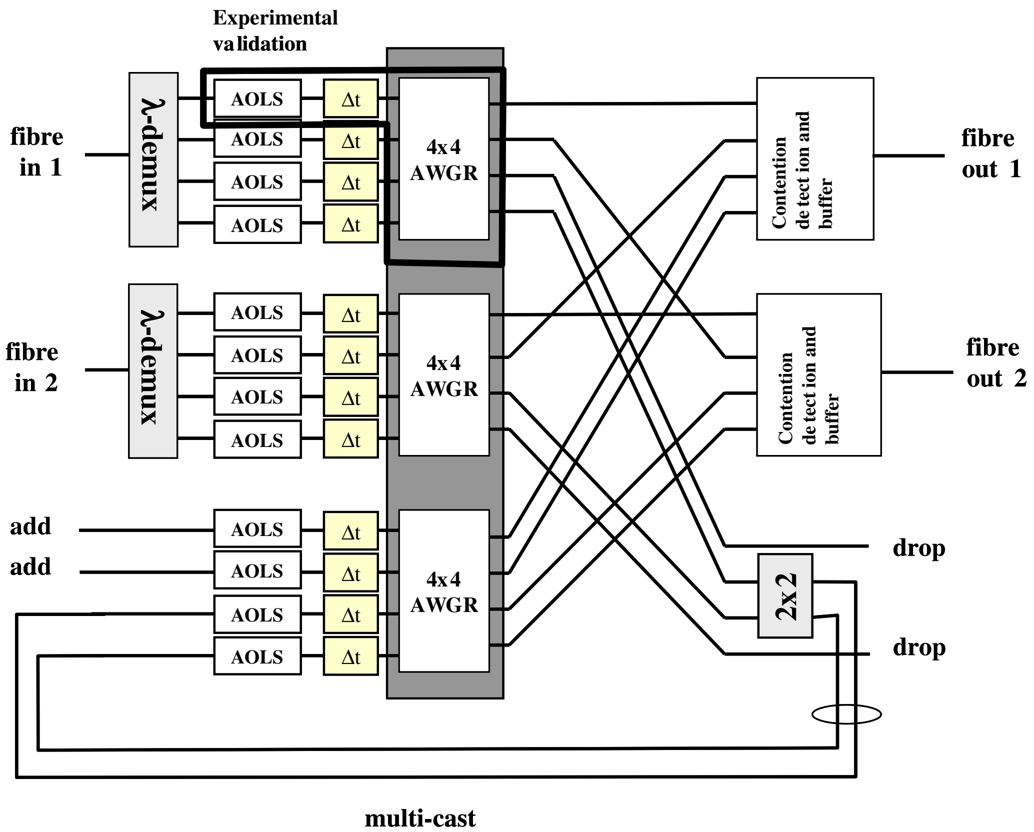

Fig. 13. LASAGNE node (photonic router).

requirements. The new address label is inserted in the output wavelength converter through modulation of the optical carrier prior to the payload. The optical header is implemented by using the SCM technique and placed in time before the payload to facilitate the header removal by simply activating an optical gate.

6.3. OPSnet switch architecture and demonstrator

The OPSnet project (Optical Packet Switched networks) investigated design issues and techniques suitable to realize a simple and fully scalable (in size and bit rate) optical packet switch, capable of operation at high bit rates beyond 100 Gb/s. The techniques used are compatible with asynchronously generated variable length packets, and can easily scale to any payload bit rates in excess of 160 Gb/s. The technical approach is as follows.

The switch node design is based on that proposed by the WASPNET project, which was developed and demonstrated by the photonic networks research laboratory in the University of Essex [18]. Fig. 12 shows a wavelength modular packet switch architecture comprising a number of switching elements placed in parallel and an advanced control mechanism that extracts the optical header and determines the required output port. Each switching element deals with packets arriving at the router on the same wavelength channel and can support switching to any output fibre at any wavelength. Space switching of the packets inside the switching element is achieved based on wavelength conversion and selection through an arrayed waveguide grating (AWG).

6.4. The all-optical label switched LASAGNE node

Fig. 13 shows the all-optical label swapping node-architecture proposed by the Lasagne project. The main functionalities such as label reading, label insertion, and packet routing are based on the use of all-optical logic gates [37,38]. These functionalities are performed by the AOLS-block (Fig. 14). The wavelengths entering the node are demultiplexed and for each wavelength an AOLS-block is implemented. Each AOLS-block applies the forwarding functionality to the incoming packets. Entering the AOLS-module, the packet payload is separated all-optically. The extracted optical label is sent to a bank of XOR autocorrelators [39], where the comparison between the label and a set of local addresses is performed. These local addresses are generated using a network of optical delay lines (ODLs). An ODL consists of a set of interconnected fibre delay lines, couplers and splitters, generating a bit sequence out of one pulse. Thus, comparing the incoming label to the local addresses implies that for each possible incoming label a separate ODL and a correlator have to be installed in the AOLS-block. After comparison, a high intensity pulse will appear at the output of the XOR correlator with the matching address. This pulse feeds a control-block that drives a wavelength converter. The control-block is made up of optical flip-flops. Depending on the matching address

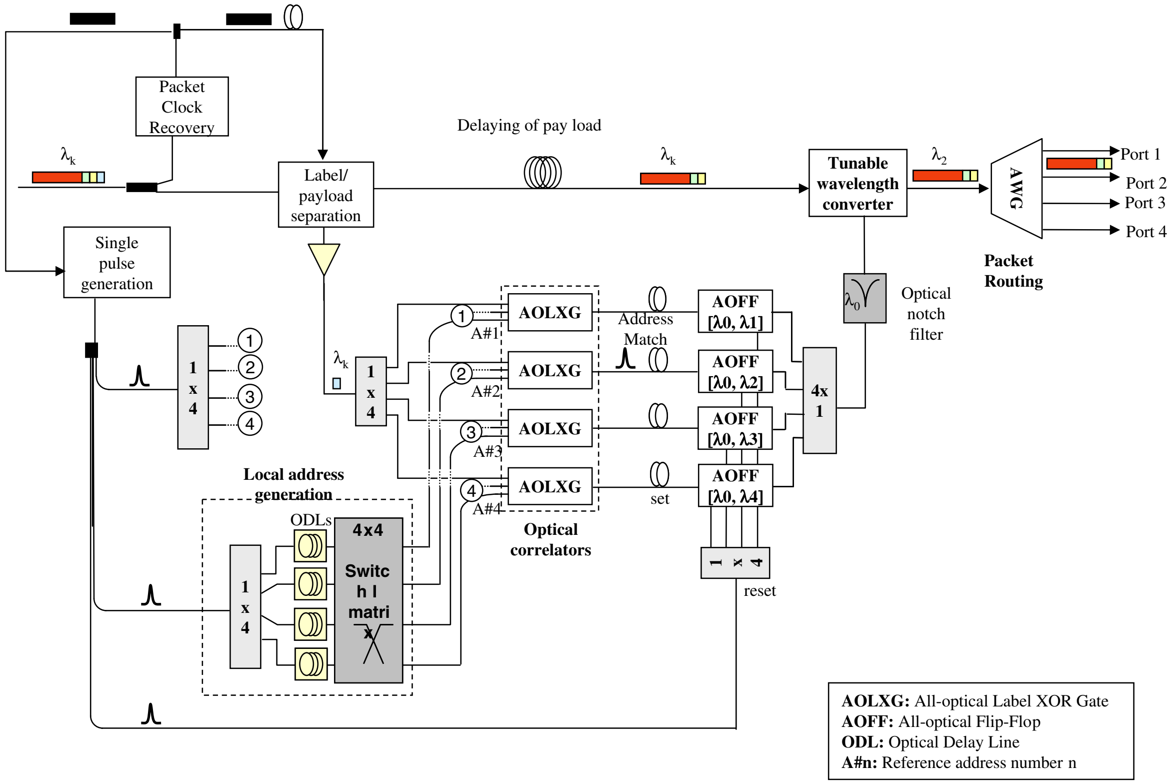

Fig. 14. Detailed LASAGNE all-optical label swapper.

(correlator output pulse), the appropriate flip-flop will emit a Continuous Wave (CW) signal at a certain wavelength. In this way, the internal wavelength is chosen. Meanwhile a new label is generated in the appropriate ODL. The new label is inserted in front of the payload and both the payload and the new label are now converted to the wavelength defined by the flip-flop [40].

The packet is then sent through an AWG (arrayed waveguide grating). Thus, the wavelength on which the packet leaves the AOLS-block determines the outgoing port on which the packet leaves the node. Two switches provide the flexibility to assign different outgoing labels and wavelengths to the same incoming label. From the AWG, packets go to the contention resolution block that belongs to their output-port. This module provides the flexibility to overcome the problems of contention in the network.

From the description of the node, it may be clear that the more labels an AOLS-block has to distinguish, the more components need to be installed. All-optical label recognition does not scale well and the use of all-optical label swapping in an optical packet-switching network creates challenges and opportunities from the networking point of view. To lower the cost of the AOLS-node, it is beneficial to reduce the number of different labels used throughout the network and hence the number of bits occupied by the label. Reduction of the number of labels does not only depends on the routing information used [41]. Even though it is very important to choose the appropriate label distribution, the network topology as well as the possibility to stack the labels affect the label length. Well thought over choices can limit the label length to 2 or 3 bits, thus only installing 4 or 8 correlators in one AOLS-block.

7. Conclusions

In this paper, recent achievements in the field of photonics in switching related to VD-S Department of e-Photon/ONe research activities, have been presented in a system perspective. The main key building blocks of optical switches have been presented to support different optical networking paradigms. An overview of the complementary expertise offered by European research groups has been outlined as a strong potential that could be turned into practical implementation and prototypes. The demonstration of the possibility to proceed with concrete applications of research results applications is given by the description of optical switching experiments ranging from hybrid short term solutions to feasible all-optical approaches.

Acknowledgement

This work has been supported by European Commission through the NoE e-Photon/ONe+ project via the Virtual Department on Optical Switching Systems (VDS).

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