OPTICAL CLOCK RECOVERY AND CLOCK DIVISION CIRCUIT

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Abstract Optical clock recovery is demonstrated from 20 Gbps pseudo-data patterns. The recovered 20 GHz clock shows 30 dB suppression of the sub-harmonics of the input data pattern, despite long series of consecutive zero's. The same circuit was also used to perform clock division by 2 and 4.

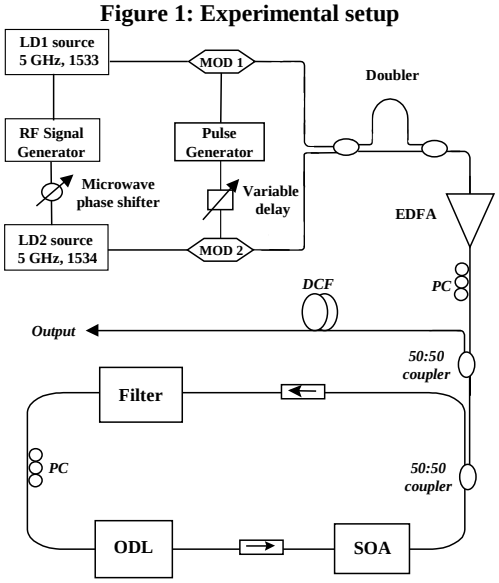
Introduction

The ability to perform clock recovery and clock division is a key requirement for high speed optical logic /1/ and regenerators circuits /2,3/. The generation of a local clock synchronized with an incoming data stream, is essential to power the optical logic gates and to provide fresh, noise-free optical signal in areas of the circuit where regeneration of the signal may be required. Similarly clock division is an important function for the receiver node, since a local clock operating at a sub-multiple of the line rate is often required to power for example a demultiplexer. So far a number of clock recovery designs have been demonstrated, using the nonlinear dynamics of a semiconductor optical amplifier (SOA) in an EDFA ring laser /4/, the phase modulation via the Kerr effect in optical fiber /5/, the nonlinear dynamics of a NOLM in a figure eight laser /6/ and a self-pulsating two-section DFB laser /7/. Recently a SOA based nonlinear loop mirror was also used for clock division /8/. In the present communication a simple circuit containing a single active device (SOA) is demonstrated. The circuit has been shown to recover clock from a data pattern up to 20 Gbps and to generate pulse trains of 4.7 ps. The same circuit has also been used for clock division from the 20 Gbps stream to 10 and 5 GHz. The recovered clock signal has been investigated for a number of data input streams, including patterns with long series of consecutive zeros.

Experiment

The concept on which the clock recovery/division circuit operates relies on the fast gain saturation and slower recovery of the intracavity SOA by external optical pulses. This concept has been recently used to demonstrate the mode-locking of a SOA fiber ring laser up to 20 GHz /9/. Figure 1 shows the experimental layout. The clock recovery circuit was constructed entirely from fiber-pigtailed devices. Gain was provided from a 500 μm, bulk InGaAsP/InP ridge waveguide SOA. The SOA could provide 23 dB small signal gain with 250 mA drive current at 1535 nm with 400 ps gain recovery time. Faraday isolators were used at the input and output of the SOA to ensure unidirectional oscillation in the ring. A 4.8 nm tunable optical filter was used for wavelength selection and a variable optical delay line (ODL) was used for precise tuning of the repetition frequency of the clock recovery circuit to the incoming data pattern. As the SOA exhibited a 2 dB polarization gain

Figure 1: Experimental setup



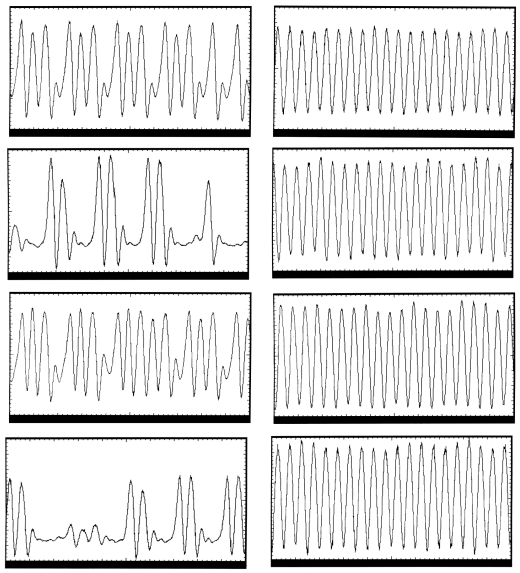
dependence, a polarization controller was introduced at its input port. A 3 dB optical fiber coupler was used after the SOA to insert the data pattern and to obtain the output from the clock recovery circuit. The programmable data sequence introduced in the recovery circuit, was constructed using two 5 GHz gain switched DFB laser operating at 1533 and 1534 nm and driven from a common RF signal generator with the addition of a variable phase shifter to time-interleave them. The pulse trains from each DFB were modulated in separate Li:NiO_3 modulators, driven from the two synchronized channels of a programmable 500 MHz pulse generator at selectable rates and duty factors to obtain various data sequences. The 20 Gbit/s signal pulse train was obtained using a split, relative delay and combine fiber doubler. At the output of the fiber doubler, the gain switched pulses were linearly compressed with dispersion

compensating fiber of total dispersion -47.5 ps/nm, to produce 12 ps pulses. Before launching into the clock recovery circuit, the signal of the final data pattern was amplified in an EDFA and its polarization state was adjusted with a polarization controller.

Results and discussion

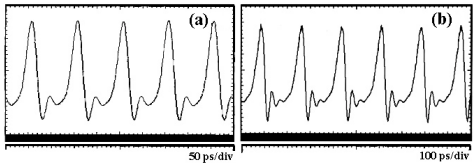
With the EDFA set to provide 400 μW in the clock recovery ring cavity and the optical delay line adjusted so that the round trip frequency of the clock recovery cavity is a subharmonic of the data repetition frequency, the laser mode-locks. Various pseudo-data patterns have been launched into the cavity by adjusting either the "on" state width of each of the modulators or the delay between them. Figure 2a shows samples of these patterns and figure 2b the corresponding output from the clock recovery circuit trains monitored on a 40 GHz sampling oscilloscope. The recovered clock signal was also monitored on a second harmonic autocorrelator, which showed a 4.7 ps pulse train at 20 GHz after compression with –11.4 ps/nm dispersion compensating fiber. The output from the circuit was also monitored on an RF spectrum analyzer and was compared to the input data pattern. This indicated that the 5, 10 and 15 GHz subharmonics of the input data signal were suppressed by 30 dB at the output of the clock recovery circuit.

Figure 2: (a) Samples of the input data sequence, and (b) corresponding recovered clock at 20 GHz. The timebase is 100 ps/div.



By electrically delaying the initial pulse trains from the DFB's by 33.3 ps, it was also possible to recover clock at 30 GHz. In this instance the pulse width of the recovered pulse train was 12 ps. Further improvements in the output pulses may be obtained by using the design guidelines for optimizing the cavity length and dispersion discussed in ref. /10/. The clock recovery circuit discussed so far is a tuned circuit that was adjusted with the variable optical delay line to mode-lock at the repetition frequency of the input data pattern. As the data input pattern possesses RF components at both 5 and 10 GHz it has also been possible to obtain clock division by adjustment of the delay line. Figure 3 (a) and (b) shows clock division by a factor 2 and 4 respectively and the pulse width of the divided clock was 4.7 ps.

Figure 3: Clock divided output at (a) 10 GHz and (b) 5 GHz.



Conclusions

We have presented an all-optical clock recovery circuit at 20 and 30 GHz. The circuit was also used for clock division to 5 and 10 GHz.

Acknowledgments

The authors would like to thank G. Guekos and H. Burkhard for providing the SOA and DFB laser devices and gratefully acknowledge partial support by the CEC via the ESPRIT program, project 36078 DO_ALL.

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